UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,796	01/07/2002	Wayne L. Cheung	IBM1P009/SJ0920010140US1	3120

28875 7590 04/15/2004

SILICON VALLEY INTELLECTUAL PROPERTY GROUP
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER	
FIGUEROA, NATALIA	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 04/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/041,796	Applicant(s) CHEUNG ET AL.	
	Examiner Natalia Figueroa	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-20* is/are allowed.

6)☒ Claim(s) *1,8 and 21* is/are rejected.

7)☒ Claim(s) *2-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Jusuf et al (USPN 6,219,195).

Regarding claim 1, Jusuf et al discloses an MR preamplifier system, comprising a magneto-resistive (MR) sensor (col. 1, lines 14-15), an alternating current (AC) coupling module (col. 34-38) couple to a direct current (DC) voltage associated with the input signal (col. 2, line 66-col. 3, line 4), a gain stage module coupled to the AC coupling module (col. 3, lines 22-24), the gain stage module including a plurality of cascode field effect transistors (FETs) configured for amplifying the input signal (col.4, lines 27-35), while reducing intrinsic noise and increasing the operational bandwidth (abstract, col. 4, line 65-col. 5, line 6),; and a control circuit to the gain stage module for feeding back an output of the gain stage module (col. 4, line 65-col. 5, line 6).

Method claim 8 is drawn to the method of using the corresponding apparatus claimed in claim 1. Therefore method claim 8 corresponds to apparatus claim 1 and is rejected for the same reasons of anticipation as used above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jusuf et al in view of Ranmuthu et al (USPN 6,396,346).

Regarding claim 21, Jusuf et al is relied upon for the same reasons of rejections as stated above. Jusuf et al fails to teach the disk drive system, comprising a magnetic recording disk; a magnetic head including a magneto-resistive (MR) sensor; an actuator for moving the magnetic head across the magnetic recording disk; and the magnetic head may access different regions of the magnetic recording disk; and a controller electrically coupled to the magnetic head including a preamplifier.

However, Ranmuthu et al disclose such sytem in (fig. 1, col.1, lines 33-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was

made to modify the apparatus as disclosed by Jusuf et al. with the above teachings from Ranmuthu et al. to include a sytem that supports given preamplifying device, hence providing different systems that will work properly at higher data rates and without errors.

Allowable Subject Matter

3. Claims 2-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 9-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim 9; the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a circuit, comprising a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to an output; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor; a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the gate terminal of the second transistor and the drain terminal of the fourth transistor; and a capacitor coupled between ground and the drain terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

Regarding claim 20; the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a circuit, comprising a first transistor including a source terminal coupled to ground, a gate terminal coupled to a first node, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal coupled to a second node, and a drain terminal coupled to a first output; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to a power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the second node; a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the second node; a sixth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to a third node; a seventh transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the second terminal of the MR sensor; an eighth transistor including a source terminal, a gate terminal, and a drain terminal coupled to a second output; a ninth transistor including a source terminal coupled to the second output, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; an operational transductance amplifier with a first input coupled to the first output and a second input coupled to the second output, the operational transductance amplifier including an output coupled to the gate terminal of the sixth transistor; a first current source including a first terminal coupled to the source terminal of the eighth transistor and a second terminal coupled to ground; a second current source including a first terminal coupled to the power source and a second terminal coupled to the gate terminal of

the fourth transistor; a first capacitor including a first terminal coupled to the power source and a second terminal coupled to the gate terminal of the sixth transistor; a second capacitor including a first terminal coupled to the second node and a second terminal coupled to ground; a third capacitor including a first terminal coupled to the first node and a second terminal coupled to the second terminal of the MR sensor; a first resistor including a first terminal coupled to the third node and a second terminal coupled to the first node; and a second resistor including a first terminal coupled to the third node and a second terminal coupled to ground.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Klein et al (USPN 5,122,915): Low-noise preamplifier. Cram (USPN 5,841,318): Low-noise preamplifier. Nainar et al (USPN 6,054,901): Low noise preamplifier. Lorenz (USPN 6,084,469): AC coupling mr-preamp. Lorenz (USPN 6,066,987): Cascode magneto-resistance preamplifier. "Low-Noise High-Bandwidth Voltage-Biasing ...", (IBM TDB): Low noise amplifier. "Low Voltage Preamp Front End Stage ...", (IBM TDB): MR head biasing. "DC MR Preamplifier with ...", (IBM TDB): MR preamplfier element. "A 0.8nV/√Hz CMOS Preamplifier ...": (IEEE): CMOS Preamplifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (703) 305-1260.

The examiner can normally be reached on Monday - Thursday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R. Hudspeth can be reached on (703) 308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NFM

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600